



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:)
Shridhar Mukund) Group Art Unit: 2128
Application No.: 10/712,711) Examiner: Lo. Suzanne
Filed: November 12, 2003) Docket No.: ADAPP222
For: SIMULATION OF COMPLEX SYSTEM) Date: January 16, 2008
ARCHITECTURE)

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450 on January 16, 2008.

Signed: _____

Justine Stamm

TRANSMITTAL OF REPLY BRIEF
IN RESPONSE TO EXAMINER'S ANSWER

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith in triplicate is the REPLY BRIEF IN RESPONSE TO EXAMINER'S ANSWER mailed January 16, 2008.

This application is on behalf of

☐ Small Entity ☒ Large Entity

Verified Statement is: ☐ Attached ☐ Already Filed

This reply brief is being filed within two (2) months of the mailing date of the Examiner's Answer. The Examiner's Answer was mailed on November 16, 2007.

If an additional extension of time is required, please consider this a petition therefor.

☒ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

☒ Charge any additional fees or credit any overpayment to Deposit Account No. 50-0805, (Order No. ADAPP222). Two additional copies of this Transmittal are enclosed.

Respectfully submitted,
MARTINE PENILLA & GENCARELLA, LLP

Jayanthi Minisandram
Jayanthi Minisandram
Reg. No. 53,330

710 Lakeway Drive, Suite 200
Sunnyvale, CA 94085
Tel: (408) 774-6905
Fax: (408) 749-6901
Customer No. 25920



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re the application of:)
Shridhar Mukund) Group Art Unit: 2128
Application No.: 10/712,711) Examiner: Lo, Suzanne.
Filed: November 12, 2003) Atty. Docket No: ADAPP222
For: SIMULATION OF COMPLEX SYSTEM) Date: January 16, 2008
ARCHITECTURE)

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on January 16, 2008.

Signed: Justine Stamm
Justine Stamm

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S REPLY BRIEF UNDER 37 C.F.R. § 41.41

Dear Sir:

Appellant submits this paper in response to the Examiner's Answer mailed November 16, 2007. The two-month period for reply extends to January 16, 2008. Accordingly, this reply is believed to be proper.

I. REPLY

A. Independent Claim 1 Is Not Properly Rejected Under 35 U.S.C. § 103(a) Since The Cited References Do Not Teach Or Suggest Block level processing

Appellant again respectfully submits that independent Claim 1 is novel and patentable over Shimogori et al. and Shridhar et al. because, for instance, the references do not suggest or teach *block level* processing wherein signals generated by a code representation are compared against signals generated by the processor circuit to identify an error and an output for display is generated to identify cause of the unacceptable comparison of the signals at a *block level* of the processor circuit, as recited in independent Claim 1. Contrary to the Examiner's assertion, the specification of the instant application implicitly provides a definition of a block as evidenced in the Background section – "Chips having large gate counts...." (meaning hardware circuit), "causes a challenge for developers ... to simulate and test the chip circuit prior to manufacturing the chip", "designs are becoming more modular, where common blocks are replicated a number of times in the chip design." A block, as implied from the aforementioned sections, may be defined as a high level (hardware) functional chip component such as memory block. (See page 2, lines 1-4, page 15, lines 1-5).

To establish a *prima facie* case of obviousness, the prior art reference(s) cited by the Examiner must, at the very least, teach or suggest all the elements of the claimed invention. MPEP § 2143; *In re Vaeck* 20 USPQ2d 1438 (Fed.Cir. 1991). The Examiner asserts that Shimogori et al. teaches processing at block level. See Examiner's Answer, mailed November 16, 2007, page 8, 3rd paragraph that states that Shimogori discloses [sic] "identifying a portion of (software) code that can be speeded up wherein blocks of code represent devices such as a memory, Shimogori identifies at a block level the cause of the unacceptable comparison of the signals and inserts a patch into a thread specific of the block level location of the error." Appellant disagrees with this assertion. As can be seen in paragraph [0090], a portion of (software) code that can be speeded up by converting to hardware, is identified, based on clock cycles consumed in various parts of the C language source code reported through an ISS profiler. Even assuming that the instant application includes software block level processing, Shimogori does not suggest or teach block level processing. Shimogori traverses through lines of C language source code and identifies a *portion of the code* that can be speeded up and replaces that *portion of the code* with hardware instructions. Shimogori does not suggest or teach

identifying the cause of the unacceptable comparison of signals at a higher block level. If, as per the Examiner, blocks of code represent devices such as memory, Shimogori does not suggest or teach identifying the cause of the error at the (memory) block level. Rather, each line of code is examined and *portions of the code* that can be speeded up are identified. This is not the same as a block level processing of the instant application wherein the cause of the unacceptable comparison of the signals at the block level is identified. If a block is determined as a memory block, the instant application identifies a specific memory block which has caused unacceptable comparison of signals and displays the location of the memory block. (See Figures 5 and 6 of the instant application where system thread 190 identifies the block level location that caused unacceptable comparison of the signals (for example, user thread 198-1 representing a specific block) and a patch is placed in the appropriate block thread, i.e. patch 206 in user thread 198-1 to further identify a signal level location of the unacceptable comparison of signals.

Further, by Examiner's own admittance in the Response to Appeal Brief, page 8, 3rd paragraph, Shimogori does not *explicitly* state "block level" processing.

B. Independent Claim 1 Is Not Properly Rejected Under 35 U.S.C. § 103(a)
Since The Cited References Do Not Teach Or Suggest identifying a cause of
unacceptable comparison of signals at a block level

Appellant again respectfully submits that independent Claim 1 is novel and patentable over Shimogori et al. and Shridhar et al because, for instance, the references do not suggest or teach identifying a cause of unacceptable comparison of signals at a *block level*, as recited in independent Claim 1. Specifically, the Examiner cites paragraph [0090] of Shimogori to support her assertion that Shimogori teaches block level processing. As mentioned above, contrary to the assertion, Shimogori does not suggest or teach block level processing. As recited in paragraph [0090], Shimogori examines clock cycles consumed by the C language source code by traversing through lines of source code as reported by the ISS system as an ISS profiler, and identifies portions of code that can be speeded up through conversion to hardware. Nowhere in the cited section or anywhere in Shimogori is there a suggestion or teaching to identify the cause of the unacceptable comparison of signals at a (higher) block level. If, as per the Examiner, blocks of code represent devices, such as memory, Shimogori does not suggest or teach identifying a block causing the unacceptable comparison of signals. Rather, upon examination of every line of code, *portions of the code* that can be speeded up are identified for conversion to hardware. This is not the same block level processing as recited in independent claim 1 of the

instant application. In the instant application, the signals generated by a code representation are compared against signals generated by the processor circuit to identify the unacceptable comparison of signals at the block level, as illustrated in Figures 5 and 6 (thread 198-1 representing a block). Upon identification of a location for the unacceptable comparison of signals at a block level, a patch (206) may be inserted into a thread specific to the identified block level to further narrow the cause of the unacceptable comparison of signals to a signal level location, as illustrated in Figure 6.

Shridhar does not suggest or teach performing a block level processing by identifying a cause of unacceptable comparison of signals at a block level. Shridhar merely suggests a process for regenerating debug commands.

The foregoing demonstrates that the cited primary references of Shimogori et al. and Shridhar et al do not alone or in combination, teach or suggest all the elements and limitations of the independent claim 1. Consequently, claim 1 and its dependent claims 2-5 are patentable.

**C. Independent Claim 6 Is Not Properly Rejected Under 35 U.S.C. § 103(a)
Since The Cited References Do Not Teach Or Suggest inserting a patch into a
thread specific to the block level location of an error**

Appellant respectfully submits that independent Claim 6 is novel and patentable over Shimogori et al. and Shridhar et al. because, the references do not suggest or teach inserting a patch into a thread *specific to the block level* location of an error, as recited in independent Claim 6. As claimed, the patch is used in further determining signal level location of the error through information generated by the patch. A general location of the error is identified at a block level using a first simulation. In order to pinpoint the exact location of the error within the identified block, a patch is inserted into a thread specific to the identified block level location of the error. The patch of the claimed invention is to further narrow the location of the error rather than *address* the error encountered.

As a result, Appellant submits that Independent claim 6 is patentable over the cited references.

**D. Independent Claim 6 Is Not Properly Rejected Under 35 U.S.C. § 103(a)
Since The Cited References Do Not Teach Or Suggest running a second
simulation for further identifying the signal level location of the error.**

Appellant respectfully submits that independent Claim 6 is novel and patentable over Shimogori et al. and Shridhar et al. because, the references do not suggest or teach running a second simulation for further pinpointing a location of the error within an identified block, as recited in independent Claim 6. Specifically, the Examiner cites paragraph [0091] of Shimogori to support her assertion that Shimogori teaches running a second simulation for further identifying the signal level location of the error. According to Shimogori, a ISS profiler is used to identify lines of code that consume clock cycles and identifying portions of code that can be speeded up through conversion to hardware. (See paragraph [0090]). Once the portions of codes are identified, the identified portions of codes are extracted and replaced with VU instructions. (See paragraph [0091]). The replacement of the portions of code by VU instructions is to *address* an “error” (consumption of clock cycles) in the code. Since the error has already been *addressed* by the “patch”, there is no reason for a second simulation to be run to further identify the location of the error. The Examiner has argued that running a second simulation is directed towards intended use of executing the simulation and that the recitation of the intended use of the claimed invention must result in a structural difference. Appellant would like to point out that the second simulation of the instant application is to further pinpoint the location of the error in a processor circuit during debugging and that the structural difference may result upon further identifying the exact location of the error from the second simulation.

The Examiner has further argued that if the prior art is capable of performing the intended use, then it meets the claim. The Appellant defers from this assertion. In order for the prior art to meet the claimed invention, the prior art must teach each and every element and limitations of the claimed invention. Specifically, the prior art must teach block level processing to identify a general location of an error in the processor circuit, insertion of a patch into a thread specific to the block level location of the error, execution of a second simulation to further narrow the location of the error (signal level location) through information generated by the patch, and correcting a code representation of a processor associated with the error. Based on the aforementioned arguments, Shimogori alone or combined with Shridhar does not suggest or teach block level processing to identify a (general) location of the error. As there is no block level processing to identify a general location of the error, there is no need for inserting a patch into a thread specific to the block level location of the error and to execute a second simulation to further narrow the location of the error within the identified block. The simulation step that the Examiner is pointing to in paragraph [0091] of Shimogori, is optional and is not a required step to further identify the location of the error within the identified block.

The Supreme Court held that “[r]jections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *KSR Intl v. Teleflex Inc.*, 82 USPQ2d 1385, 1397 (U.S. 2007) (citing *In re Kahn*, 78 USPQ2d 1329 (CA Fed. 2006). Moreover, the Court held that to facilitate a review of whether a patent claiming a combination of elements of prior art is obvious; the analysis “should be made explicit.” *Id.*

The Examiner asserts that it would have been obvious to arrive at the claimed invention using the teachings of the primary references as Shimogori in combination with Shridhar is capable of performing the intended use. See Examiner’s Answer, mailed November 16, 2007, at page 10. Assuming arguendo that one of ordinary skill would have been motivated to combine the cited references as asserted by the Examiner, there is still no explicitly articulated reason provided by the Examiner to support how the cited combination of references teach block level processing, installing a patch into a thread specific to the block level location of an error, running a second simulation to pinpoint the location of the error and providing corrections to address the error. As previously discussed, Shimogori et al. merely teach identifying a portion of code that can be speeded up and replacing the identified portions of code with VU instructions (hardware). See Shimogori et al. paragraph [0090] and [0091]. Moreover, no where does Shridhar et al. mention identifying a block level location having an error, inserting a patch to narrow the location of the error within the identified block and running a second simulation to further narrow the location of the error.

The foregoing demonstrates that there is simply no reason having some rational underpinning to support obviousness based on the cited primary references of Shimogori et al. and Shridhar et al. Consequently, independent Claims 1, 6 and Claims 2-5 and 7-14 which respectively depend therefrom are patentable.

Independent Claim 15 Is Not Properly Rejected Under 35 U.S.C. § 103(a) For At Least The Same Reasons Stated With Respect To Independent Claim 1


Shimogori et al. and Shridhar et al., as discussed above regarding independent Claim 1, do not teach or suggest identifying a cause of unacceptable comparison of signals at a *block level*, as recited in independent Claim 15. Therefore, similar remarks as those presented above regarding Claim 1 also apply with equal force to independent Claim 15.

Accordingly, for at least the reasons stated above regarding the Applicant's submission that independent Claim 1 is patentable over Shimogori et al. in view of Shridhar et al., independent Claim 15 and Claims 16-19 which respectively depend therefrom are likewise patentable over Shimogori et al. in view of Shridhar et al.

II. CONCLUSION

In view of the foregoing arguments distinguishing Claims 1-19 over the art of record, Appellant respectfully submits that the claims are in condition for allowance, and respectfully request that the rejection of these claims be reversed.

Respectfully submitted,
MARTINE PENILLA & GENCARELLA, L.L.P.


Jayanthi Minisandram
Reg. No. 53,330

Martine Penilla & Gencarella, LLP
710 Lakeway Drive, Suite 200
Sunnyvale, California 94085
Telephone: (408) 774-6920
Customer Number 25920